REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 15-19, 23-24, and 26-38 are in this application. Claims 1-14, 20-22, and 25 have been cancelled. Claims 15-19, 23-24, and 26 have been amended. Claims 27-38 have been added to alternately claim the present invention. In addition to the amendments discussed below, the claims have also been amended to broaden the claims, and alternately recite the present invention. Further, the specification has been amended to delete the "Summary of the Invention" section.

The present divisional application was filed with copies of the 20 informal sheets of drawings that were originally filed in the parent application, along with 20 sheets of formal drawings. As a result, it is not clear which set of drawings (informal or formal) has been approved by the Examiner. Thus, applicant requests that 20 informal sheets and the 20 formal sheets of drawings filed with the divisional application be replaced with the 20 replacement sheets attached in Appendix A. The 20 sheets of replacement drawings are the same as the formal drawings filed with the divisional application.

The Examiner rejected claims 15 and 21 under 35 U.S.C. §102(a) as being anticipated by applicant's admitted prior art. For the reasons set forth below, applicant respectively traverses this rejection.

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Claim 15 has been amended and recites:

"A method of forming a plurality of semiconductor devices in a semiconductor material having a first semiconductor region of a first conductivity type, a second semiconductor region of a second conductivity type, and a third semiconductor region of the second conductivity type, the method comprising:

"simultaneously doping the first semiconductor region and the second semiconductor region while protecting the third semiconductor region from being doped; and

"simultaneously doping the second semiconductor region and the third semiconductor region while protecting the first semiconductor region from being doped."

Applicant is respectfully unclear as to the rejection set forth by the Examiner as the Examiner read two different structures to be the second region required by claim 15. In discussing the first element of claim 15, the Examiner pointed to p-well 134 shown in applicant's prior art FIG. 1 as constituting the first (semiconductor) region, and p-well 132 as constituting the second (semiconductor) region. In then discussing the second element of claim 15, the Examiner pointed to n+ region 144 shown in applicant's prior art FIG. 1 as constituting the second (semiconductor) region, and p-well 130 as constituting the third (semiconductor) region. As a result, applicant is unclear as to which structure (p-well 132 or n+ region 144) the Examiner has read to be the second (semiconductor) region.

However, from what can be determined, there is nothing in applicant's admitted prior art that teaches or suggests the first "simultaneously doping" element required by claim 15. In the first simultaneously doping element, a first semiconductor region (e.g., an n-type region) and a second semiconductor region (e.g., a p-type region) must be doped, while a third semiconductor region (e.g., a p-type region) is protected from being doped.

With reference to applicant's FIG. 1B, assume that n+ region 144 is read to be the first semiconductor region required by claim 15, and p-well 132 is read to be

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the second semiconductor region required by claim 15. Even if it were then assumed (only for the sake of argument) that the dopant introduced into p-well 130 and p-well 132 is also introduced into n+ region 144, there is no p-well which can be read to be the third semiconductor region required by claim 15 because there is no p-well which is protected from being doped. As shown in applicant's FIG. 1B, p-wells 130 and 134 also are doped and therefore cannot be read to be the third semiconductor region.

Thus, since applicant's admitted prior art does not teach or suggest the first "simultaneously doping" element, claim 15 is not anticipated by applicant's admitted prior art. (As noted above, claim 21 has been cancelled.)

The Examiner also rejected claims 16-17 and 22-23 under 35 U.S.C. §103(a) as being unpatentable over applicant's admitted prior art in view of Muramoto et al. (U.S. Patent No. 6,198,140). In rejecting the claims, the Examiner appears to argue that applicant's admitted prior art teach all of the limitations of claim 15. However, as noted above, claim 15 is not anticipated by applicant's admitted prior art. Thus, since claims 16-17 and 23 depend either directly or indirectly from claim 15, claims 16-17 and 23 are patentable over applicant's admitted prior art in view of Muramoto for the same reasons that claim 15 is not anticipated by applicant's admitted prior art. (As noted above, claim 22 has been cancelled.)

New claim 28 recites, in part:

"simultaneously doping the channel region of the first semiconductor region and the channel region of the second semiconductor region to define a threshold voltage in the channel region of the first semiconductor region, and partially define a threshold voltage in the channel region of the second semiconductor region."

From what can be determined, there is nothing in applicant's admitted prior art that teaches or suggests this limitation. As a result, claims 28-38 are patentable over applicant's admitted prior art.

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The Examiner objected to claims 18-20 and 24-26, but indicated that these claims would be allowable if rewritten to be in independent form including all of the limitations of the base claim and any intervening claims. Claims 18-20 and 24-26 have not been rewritten to be in independent form at this time in view of the above amendments.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

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APPENDIX A